40. (New) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric.

41. (New) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

42. (New) The method according to claim 39, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm.

43. (New) The method according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels upon a contact landing pad.

44. (New) The device according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

45. (New) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

46. (New) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

47. (New) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.